DASIA 2019

Torremolinos June 4 -6

PROGRAMME

MELIÃ
COSTA DEL SOL

MÁLAGA

EUROSPACE

In co-ordination with:

esa

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9:45	**Conference intro by the DASIA Chairman**

A1: Cables & Wires - Chair: B. Dellandrea, Thales Alenia Space

10:15	New Antistatic, Atomic-Oxygen Resistant And High Performance Low Mass Wires And Cables Solutions For Space Applications. ***Presenter: P-Y. Mikus, Axon Cable***

A2: SpaceWire & SpaceFibre - Chair: B. Dellandrea, Thales Alenia Space France

10:45	SpaceWire and SpaceFibre Network Study - ***Presenter: V. Kollias, Teletel SA***
11:15	Designing spacewire networks with the latest generation of test and development equipment - ***Presenter: D. Gibson, STAR-Dundee***

A3: SpaceFibre - Chair: U. Hoch, Airbus Defence & Space GmbH

11:45	An Investigation on SpaceFibre Protocol Maturity: Interopeability Tests - ***Presenter: P. Nannipieri, University of Pisa***
12:15	SpaceFibre Implementation Performance Assessment: Simulation & Traffic Generation at full network load - ***Presenter: V. Kollias, Teletel SA***

13:00 Lunch

A3: SpaceFibre cont.

14:00	SpaceFibre Routing Switch IP Implementation in Radiation-Tolerant FPGAs - ***Presenter: A. Gonzales Villafranca, STAR-Barcelona***

A4: Network & Sensor Platforms - Chairman: G. Lautenschläger, Airbus Defence & Space GmbH

14:30	GRCANFD_CAN-FD controller with DMA engine and AHB or AXI interface - ***Presenter: J. Espana-Navarro, Cobham Gaisler AB***
15:00	TT-EPOS - a Modular Time Triggered Ethernet Platform for Outer Space - ***Presenter: D. Jelem, TTTech Computertechnik AG***

15:30 Coffee break

A4: Network & Sensor Platforms cont

16:00	High-performance, high availability and high-reliability Interconnect for Spaceflight Applications - ***Presenter: A. Gonzales Villafranca, STAR-Barcelona***
16:30	Decentralised Subsystem Control using Rad-hard Microcontrollers - ***Presenter: S. Duncan - Thales Alenia Space UK***

A5: COTS based OBC's - Chair: J-L. Poupat, Airbus Defence & Space SAS

17:00	Fault Tolerant and COTS based On-board Computer for Small Satellites - ***Presenters: A. Avanzi & G. Tuccio, Sitael SpA***
17:30	Highly Reliable COTS Satellite and Launcher Computers - ***Presenter: P. Sandin, Ruag Space AB***

June 4
Room B

9:45 **Conference intro by the DASIA Chairman**

B1: Memory-Controllers - Chair: F. Siegle, ESA/ESTEC

10:15 Improving Multicore Performance with a new DDR2 and DDR3 SDRAM - ***Presenter: D. Hellstrom, Cobham Gaisler AB***

10:45 RIMC DDR3_DDR3 controller and Radiation Mitigation. ***Presenter: B. Huret, 3D Plus***

B2: OS Frontends- Chair: A. Rossignol, Airbus Defence & Space SAS

11:15 Improved Clang/LLVM toolchain for LEON3_4 ***- Presenter: D. Hellstrom, Cobham Gaisler AB***

11:45 Opportunities and challenges for embedded Linux ***- Presenter: A. Certain, Airbus Defence & Space SAS***

B3: Multicore Processors & Hypervisors 1 - Chair: D. Hellstrom, Cobham Gaisler AB

12:15 Towards a Dependable Parallelism for Real Time Systems - ***Presenter: E. Jenn, IRT Saint-Exupery***

13:00 Lunch

B3: Multicore Processors & Hypervisors 1 cont.

14:00 Multicore Processors and Hypervisors_ a great opportunity for embedded real-time systems - ***Presenter: O. Notebaert, Airbus Defence & Space SAS***

14:30 GXtratuM, a Qualified hypervisor for space: applications: Current status and future perspective - ***Presenter: P. Gómez Molinero, Fentiss S.L.***

B4: Multicore Processors & Hypervisors 2 - Chair: M. Prochazka/J. Fuchs, ESA/ESTEC

15:00 Porting the Air TSP to the Arm Architecture with the Miura1 Obsw as Use Case - ***Presenter: L. Murta, GMV Skysoft S.A.***

15:30 Coffee break

B4: Multicore Processors & Hypervisors 2 cont

16:00 XtratuM adaptation for Low-Power Real-Time - ***Presenter: A.Crespo, Fentiss S.L.***

16:30 Understanding interference in critical multicore systems - ***Presenter: H. Ghazzawi, Rapita Systems Ltd.***

B5: MBSE & CASE - Chair: R. Gerlich, BSSE

17:00 Model-based methodology for space vehicles ***- Presenter: S. Zverlov, Fortiss***

17:30 Numerical Reproducibility for Model-Based Software Engineering - ***Presenter: A. Arregi, GTD Gmbh***

A5: COTS based OBC's cont - Chair: J-L. Poupat, Airbus Defence & Space SAS

09:00	COTS Based Reliable Architecture (COBRA) - ***Presenter: M. Rimpault, Airbus Defence & Space SAS***

A6: ARM based solutions - Chair: H-J. Herpel, Airbus Defence & Space GmbH

09:30	New Rad-hard Embedded Developments for Space Applications - ***Presenter: R. Bannatyne, VORAGO Technologies***
10:00	DAHLIA, Very High Performance Microprocessor for Space Applications - ***Presenter: J-L. Poupat, Airbus Defence & Space SAS***

10:30 Coffee Break

A6: ARM based solutions - Chair: O. Notebaert, Airbus Defense and Space SAS

11:00	Introduction of Quad ARM® Cortex® A72 Processor & Qormino® Common Compute Platform for Space applications, and de-risking the use of such technology into Space - ***Presenters: T. Guillemain & M. Ball, Teledyne e2v***
11:30	Lynx – Very High Performant and Flexible Processing Boards - ***Presenter: P. Sandin, Ruag Space AB***
12:00	Microchip ARM Solutions for Space Rad Hard & Rad Tolerant ARM SoC with space software ecosystem - ***Presenters: M. Mosdorf, N 7 Space Sp. z.o.o. with N. Ganry, Microchip Technology France***

13:00 Lunch

A7: OBC structures & systems - Chair: A. Fernandez-Leon, ESA/ESTEC

14:00	Development of High Flexibility On-Board Computer : ***Presenter: YunKi Lee, KARI***
14:30	Centralized OBC - ***Presenter: J. Galizzy, CNES***
15:00	FUSIO RT update: a complete European Space Computer Core, Ready to use - ***Presenter: C. Dang Feller, 3D Plus***

15:30 Coffee break

16:00 - 18:00

Panel Session: Large FPGA/VHDL Qualification

Panel members: B. Dellandrea (chair), J. Fuchs, A. Rossignol. K. Marinis, T. Helfers.

Panel members have very short presentations – max. 10 Min. - dispersed over the panel session with discussion in forum between presentations.

Panel members will stimulate discussion in Forum.

Panel Focus: Refer separate description "Focus of Panel on Large FPGA/VHDL Qualification" (please click here)

Gala dinner and entertainment hosted by Eurospace
Meeting time and point : 20:00 near the central outdoor swimming pool

B5: MBSE & CASE cont - Chair: R. Gerlich, BSSE

09:00	SAVOIR EDS_A digital capability for avionics architecture co-design. ***Presenter: M-H. Deredempt, Airbus Defence & Space SAS***
09:30	Automated Validation Testing of Ariane 6 Flight Software - ***Presenter: I. Eballard, ArianeGroup***

B6: Requirements, Validation, Testing & Simulators - Chair: C. Joergensen, Terma A/S

10:00	Code Coverage on Space Embedded Systems with GCOV - ***Presenter: L. Murta Mendes, GMVIS Skysoft S.A.***

10:30 Coffee Break

B6: Requirements, Validation, Testing & Simulators cont

11:00	Automation of Requirements-based Testing - ***Presenter: R. Gerlich, BSSE***
11:30	Early validation of requirements - a step towards better specifications - ***Presenter: H-J. Herpel, Airbus Defence & Space GmbH.***
12:00	Increasing Representativeness of SIL V&V Simulators - ***Presenter: L. Murta Mendes, GMVIS Skysoft S.A.***

13:00 Lunch

B7: Avionics Data Hdl. Systems: CORA - Chair: U. Hoch, Airbus Defence & Space GmbH

14:00	Compact Reconfigurable Avionics – Reconfigurable Data Handling Core - ***Presenter: A. Samuelsson, Cobham Gaisler AB***
14:30	CORA-MBAD: A model based avionics design environment for HW/SW co-design - ***Presenter: P. Lopez Cueva, Thales Alenia Space***
15:00	CoRA Smart AOCS&GNC Elements (SAGE) - ***Presenter: A. Figueroa González, SENER***

15:30 Coffee break

16:00 - 18:00

Panel Session: Large FPGA/VHDL Qualification

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Meeting time and point : 20:00 near the central outdoor swimming pool

A7: OBC structures & systems cont - Chair: A. Fernandez-Leon, ESA/ESTEC

09:00	The New Generation SAVOIR On-Board Computer - ***Presenter: P. Sandin, Ruag Space AB***
09:30	IPAC: On Board Computer based on the LEON4 multicore processor and XtratuM hypervisor - ***Presenter: C. Paccagnini, Thales Alenia Space***

A8: Hig Perf. OB Data Hdl-Systems - Chair: C. Paccagnini, Thales Alenia Space Italy

10:00	MIURA 1: Data Handling System - ***Presenter: M. Melara, GMV Aerospace & Defense SAU***

10:30 Coffee Break

A8: High Perf. OB Data Hdl-Systems cont

11:00	Next Generation Data Handling System – OBC-SA / SPINAS (On Board Computer – System Architecture / SPace INfrastructure and Software) - ***Presenter: T. Hartmann, Airbus Defence and Space GmbH***
11:30	High Performance Data Processor (HPDP) – A New Generation Space Processor in Demonstration - ***Presenter: T. Helfers, Airbus Defence & Space GmbH***
12:00	On-board data handling system for small modular earth observation satellites - ***Presenter: T. Hartmann, Airbus Defence & Space GmbH***

13:00 Lunch

A9: High Perf. OB Image & EO systems - Chair: S. Duncan, Thales Alenia Space UK

14:00	Hardware Accelerated Visual Localisation For Next Generation Mars Rovers - ***Presenter: D. Townson, Scisys Ltd UK***
14:30	Efficient Image Data Processing for the JANUS Instrument on JUICE - ***Presenter: B. Fiethe, Institute of Computer and Network Engineering (IDA)***
15:00	GPU4S: Towards Embedded GPUs in Space - ***Presenter: L. Kosmidis, Barcelona Supercomputing Center***
15:30	Software defined earth observation satellite with RC64 - ***Presenter: P. Aviely, Ramon Chips***

16:00 Chairman's conclusions

B8: S/C Constellation Operations - Chair: J. Fuchs, ESA/ESTEC

09:00 Using maintenance data to provide consolidated Galileo system availability - ***Presenter: M. Bieber, ESA/ESTEC***

09:30 Tricks to extend the lifetime of the CLUSTER S/C - ***Presenter: G. Lautenschläger, Airbus Defence & Space GmbH***

B9: Avionic Systems - Chair: P. Cormery, Ariane Group France

10:00 DARWIN Centralized And Modular Avionic Architecture - ***Presenter: C. Sinibaldi, CNES***

10:30 Coffee Break

B9: Avionic Systems cont

11:00 An Ethernet-based architecture for launcher avionics - ***Presenter: B. Regnier, CNES***

11:30 An end-to-end flight operating system using Micropython and the Basilisk software testbed - ***Presenter: M. Cols Margenet, University of Colorado Boulder***

12:00 Performance and power consumption analysis of new system-on-chip processing avionics for space applications - ***Presenter: M. Melara, GMV Aerospace & Defence SAU***

13:00 Lunch

B9: Avionic Systems cont

14:00 The Euclid High Gain Antenna Control Logic Verification ***Presenter: F. Simeoni, Thales Alenia Space Italy***

B10: High Perf. Payload Systems incl. Robotics - Chair: J-C. Damery, CNES

14:30 A Compact High-Performance Payload Data Handling Unit - ***Presenter: U. Kulau, DSI Aerospace Technologie***

15:00 One approach to multicore programming for payload data processing - ***Presenter: H-J. Herpel, Airbus Defence & Space GmbH***

15:30 Design of a self-adaptive, self-healing MPSoC architecture targeting robotic applications through CERBERO tools and technologies - ***Presenter: P. Sánchez de Rojas Méndez, Thales Alenia Space Spain***

16:00 Chairman's conclusions (in Room A)

Focus of Panel on Large FPGA/VHDL Qualification

Recent technology improvements have allowed manufacturing high capacity and highly re-configurable FPGAs for the space domain. The high capacity of these new FPGAs has allowed manufacturers to include hard-coded processors on their FPGAs and integrating a group of large VHDL IPs within a single chip, thus creating the possibility of having a highly integrated but also reconfigurable execution platform, constituing a true System On Chip.

Most next generation space computers will make use of these designs. However, in order to take full advantage of them, the engineering methodology has to be adapted, leaning towards HW/SW co-design methodologies and adapting the current processes for VHDL development, verification and qualification.

Many points need to be investigated further to support future development and optimize the capabilities of the space business to make the best benefit of such technologies:

- One of the most important decisions during HW/SW co-design is partitioning between the software and hardware parts. Tools are needed to help to perform the tradeoff between the possible architectures, allowing rapid prototyping and verification,
- One way of doing it is to automate as much as possible the implementation of the different elements, allowing a quick deployment and verification of the requirements.
- Embedding a group of IPs within a single VHDL code raises the question of maintenance of the blocks and possibilities for partial reconfiguration without redesigning the full code; hence space segregation of IPs and multiple access capabilities along with partial reconfigurations/ dynamic patching will get more and more important as the IPs integration will be growing
- Verifying the behaviour of a realtime software in a CPU presents a challenge, the VDHL execution within the FPGA will raise the same level of concerns: Processes for monitoring the execution of large IPs will need to be defined in order to enable debugging the VHDL on-target during Ground testings, and possibly in Space monitoring
- There is no consensus yet about which development and qualification process and standards we can define or adapt and apply for such devices and applications, this will need a standardized approach at ESA level as a minimum

LOCATION

Meliá Costa del Sol

Paseo Marítimo, 11, 29620 Torremolinos
Málaga, Spain

https://www.melia.com/en/hotels/spain/torremolinos/melia-costa-del-sol/index.htm

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REGISTRATION

Advance

Please contact us at **dasia2019@eurospace.org i**n order to get the electronic Conference Registration Form and send it to Eurospace before April 30th, 2019. This applies both to participants and to the booking of stands.

On site

The Conference Secretariat will open in the morning on June 4th, 2019 at 8:00 for late conference registration and for arrival registration and handout of conference material including a USB-stick with the program and related abstracts.

CONFERENCE FEES

A Conference fee of 940 € is requested from all participants, including speakers and chairmen.
This fee will include lunches, coffee breaks, gala dinner and handling of proceedings.
Students are kindly asked to contact Eurospace before making any registration at **dasia2019@eurospace.org**
The fee for a **Vendor Display** is **2 500 €** and includes one attendance fee for the Conference.
Conference fee of 940 € is requested from all participants, including speakers and chairmen.

PAYMENT

Cheque

French banks only: in Euro to the order of EUROSPACE payable in a French Bank to be sent to: **EUROSPACE, 15/17 avenue de Ségur 75007 Paris.**

Cash

In Euro at the Conference

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Charges on bank orders shall be borne by the sender

HOTEL RESERVATION

A block reservation has been made at special conference rates at Melia Costa Del Sol hotel.
After March 31st , reservations will be on normal request and upon availability.

CANCELLATION

Refunds of 50% will be made if a written request is received **before May 4th, at the latest.**
No refunds will be made for cancellations received **after this date,** but substitutions will be possible.

LANGUAGES

English will be the working language of the Conference. The time allocated for each presentation will include a discussion at the end

PAYMENT & BANK FACILITIES

Travel and exchange arrangements can be made by the Concierge of the Hotel.

PROCEEDINGS

Until **1st of July 2019** authors will have the opportunity to convert their abstract into a final paper to be inserted into the Eurospace DASIA 2019 Archive. In addition the insertion into the archive of the presentation prepared for the conference is very welcome.

The archive will be accessible with a common password for all conference participants and Program Board members. This password can be given to colleages and other interested parties.

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Presentations and Panels

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